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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/732,970	12/11/2003	Theodore W. Houston	TI-35974	8532

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EXAMINER	
PHAN, TRONG Q	
ART UNIT	PAPER NUMBER
2827	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/732,970	HOUSTON, THEODORE W.
	Examiner	Art Unit
	TRONG PHAN	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-16 and 18-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-16 and 18-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-4, 6-16 and 18-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Deng et al., 6,925,025 (it should be noted that there is another inventor Xiaowei Deng as set forth in item (1) of 35 USC 102(e)).

Deng et al., 6,925,025, discloses in Fig. 1 a SRAM device comprising:

Regarding claims 1, 6-7, 9-10, 14, 18-19, 21-22, 24 and 28-30:

SRAM array 110;

immediate column peripheral circuitry 152;

sleep mode power down voltage controller 170 may include a diode-bridged header or a low drop-out (LDO) voltage regulator to regulate a high supply voltage VDDM of 0.9V that is lower than high operating voltage VDD of 1.2V by a voltage drop across the header-diode 125 and a low supply voltage VSSM of 0.3V that is higher than low operating voltage VSS of 0V by the voltage drop across the footer-diode 129 (see lines 58-63, column 5 and lines 17-35, column 6) provided to SRAM array 110 during the sleep mode;

wherein:

sleep mode power down voltage controller 170 **must provide concurrently** the high supply voltage VDDM and the low supply voltage VSSM to SRAM array 100 during the sleep mode in order to establish the boundary in the SRAM device which is an interface that occurs between two different voltage domains (see lines 52-53, column 3);
sleep mode power down voltage controller 170 can control voltage for the peripheral circuitry and the SRAM array to reduce current leakage during the sleep mode (see lines 29-34, column 3) in which the current leakage is often primarily based on the parameters of the SRAM cell transistors (see lines 24-27, column 2; lines 59-67, column 3), therefore, the high supply voltage VDDM and the low supply voltage VSSM to SRAM array 100 provided from the sleep mode power down voltage controller 170 during the sleep mode are inherently based on the transistor parameter of at least one transistor of the SRAM array;

Regarding claims 2-4:

the data in the SRAM array may be maintained by the diode-limited voltages VDDM and VSSM with the n-well voltage at about high operating voltage VDD of 1.2 V (see lines 31-34 and 41-42, column 6), therefore, sleep mode power down voltage controller 170 provides the high supply voltage VDDM and the low supply voltage VSSM **relative** to the n-well voltage to SRAM array 100;

Regarding claims 8, 11, 23 and 31:

the voltages VDDM and VSSM may have values at approximately 0.9 volts and 0.3 volts, respectively, in the sleep mode and the n-well of the SRAM array 110 may be

held at approximately 1.2 volts (see lines 28-31, column 6), therefore, the SRAM array may have about 0.3 volts back bias on both n-channel and the p-channel transistors in addition to about the same voltage of 0.3 volts across the SRAM cell to provide a set of optimum values for a general technology class of transistors;

Regarding claims 12-13 and 25:

to reduce the current leakage, the battery-powered wireless apparatus may power down the row and column circuitry associated with the memory array and enter the sleep mode while still supplying sufficient voltage across the memory array to retain data (see lines 24-31, column 2);

Regarding claim 27:

low operating power supply voltage VSSM must be higher than a substrate voltage during the sleep mode even if the substrate voltage is not shown of is described in Deng et al., 6,925,025. However, it is very well known in the art that in any memory integrated circuit the base substrate voltage must be lower than any operating power supply voltage during any operation.

Response to Arguments

7. Applicant's arguments filed on 7/13/06 have been fully considered but they are not persuasive because of the following reasons:

a) Deng et al., 6,925,025, does teach the sleep mode power down voltage controller 170 can control voltage for the peripheral circuitry and the SRAM array to reduce current leakage during the sleep mode (see lines 30-34, column 3), however, the current leakage is often from the SRAM cell transistors (see lines 24-27, column 2),

therefore, the high supply voltage VDDM and the low supply voltage VSSM to SRAM array 100 provided from the sleep mode power down voltage controller 170 during the sleep mode are inherently based on the transistor parameter of at least one transistor of the SRAM array;

b) Deng et al., 6,925,025, does teach the data in the SRAM array may be maintained by the diode-limited voltages VDDM and VSSM with the n-well voltage at about high operating voltage VDD of 1.2 V (see lines 31-34, column 6), therefore, sleep mode power down voltage controller 170 provides the high supply voltage VDDM and the low supply voltage VSSM **relative** to the n-well voltage to SRAM array 100;

c) the voltages VDDM and VSSM may have values at approximately 0.9 volts and 0.3 volts, respectively, in the sleep mode and the n-well of the SRAM array 110 may be held at approximately 1.2 volts (see lines 28-31, column 6), therefore, the SRAM array may have about 0.3 volts back bias on both n-channel and the p-channel transistors in addition to about **the same** voltage of 0.3 volts across the SRAM;

d) Deng et al., 6,925,025, does teach the voltages VDDM and VSSM may have values at approximately 0.9 volts and 0.3 volts, respectively, in the sleep mode and the n-well of the SRAM array 110 may be held at approximately 1.2 volts (see lines 28-31, column 6), therefore, the SRAM array may have about 0.3 volts back bias on both n-channel and the p-channel transistors in addition to about the same voltage of 0.3 volts across the SRAM cell to provide **a set of optimum values for a general technology class of transistors;**

e) Deng et al., 6,925,025, does teach to reduce the current leakage, the battery-

powered wireless apparatus may power down the row and column circuitry associated with the memory array and enter the sleep mode while still supplying sufficient voltage across the memory array to retain data (see lines 24-31, column 2);

f) Deng et al., 6,925,025, does teach low operating power supply voltage VSSM must be higher than a substrate voltage during the sleep mode even if the substrate voltage is not shown in Deng et al., 6,925,025. Furthermore, it is very well known in the art that in any memory integrated circuit the base substrate voltage must be lower than any operating power supply voltage during any operation;

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG PHAN whose telephone number is (571) 272-1794. The examiner can normally be reached on M-F (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on (571)272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phan Trong

TRONG PHAN
PRIMARY EXAMINER